

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

10

Applicant : Paul Strong, et al.

App. No. : 09/802,046

Filed : March 8, 2001

For : **METHOD AND APPARATUS
FOR ENHANCING THE
PERFORMANCE OF A
PIPELINED DATA
PROCESSOR**

Examiner : Unknown

Group Art Unit: 2123



27299

PATENT TRADEMARK OFFICE

I hereby certify that this correspondence and all marked attachments are being deposited with the United States Postal Service as first-class mail in an envelope addressed to: Assistant Commissioner for Patents, Washington, D.C. 20231, on

Friday, August 16, 2002
(Date)

Robert F. Gazdzinski, Reg.
No. 39,990

TRANSMITTAL LETTER

Assistant Commissioner for Patents
Washington, D.C. 20231

Dear Sir:

Enclosed for filing in the above-identified application are:

1. Information Disclosure Statement (2 pages);
2. Form PTO-1449 (1 page) listing twelve (12) references, which are enclosed;
3. Copy of International Search Report (10 pages); and,
4. Return prepaid postcard.

The Commissioner is hereby authorized to charge any additional fees under 37 CFR 1.16 and 1.17 that may be required, or credit any overpayment to Deposit Account No. 501423. A duplicate copy of this sheet is enclosed.

Respectfully submitted,

GAZDZINSKI & ASSOCIATES

Dated: 8/16/02

By:

Robert F. Gazdzinski, Attorney of Record
Registration No. 39,990
11440 West Bernardo Court, Suite 375
San Diego, CA 92127
Telephone: (858) 675-1670
Facsimile: (858) 675-1674

RECEIVED
AUG 21 2002
Technology Center 2100



PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant : Paul Strong, et al.)
App. No. : 09/802,046)
Filed : March 8, 2001)
For : **METHOD AND APPARATUS FOR**)
ENHANCING THE)
PERFORMANCE OF A)
PIPELINED DATA PROCESSOR)
Examiner : Unknown)
Group Art Unit: 2123)



27299
PATENT TRADEMARK OFFICE

RECEIVED

AUG 21 2002

Technology Center 2100

INFORMATION DISCLOSURE STATEMENT

Assistant Commissioner for Patents
Washington, D.C. 20231

Dear Sir:

Enclosed is form PTO-1449 listing twelve (12) references that are also enclosed. Pursuant to 37 C.F.R. 1.97(b)(3) this Information Disclosure Statement is being filed before the mailing date of a first Office Action. Applicants note that the information contained in the attached PTO-1449 form was cited in a communication from a foreign patent office in a counterpart foreign application; a copy of the International Search Report is attached for your reference. Note that several of the references cited on the aforementioned search report were previously cited in the IDS dated November 5, 2001.

App. No. : 09/802,046
Filed : March 8, 2001

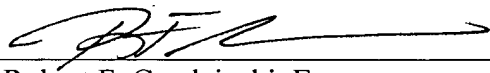
If a first Office Action on the merits was mailed before the mailing date of this Statement, it is requested that the Commissioner charge any fees under 37 C.F.R. § 1.16 and 1.17 to Deposit Account No. 501423.

Pursuant to 37 C.F.R. § 1.97(g) and (h), Applicant makes no representation that a search has been made or that the information cited is considered to be material to patentability. Additionally, inclusion on this list is not an admission that any of the cited documents are prior art in this application. Further, Applicant makes no representation regarding the completeness of this list or that better art does not exist.

Respectfully submitted,

GAZDZINSKI & ASSOCIATES

Dated: 8/16/02

By: 

Robert F. Gazdzinski, Esq.
Registration No. 39,990
Attorney of Record
11440 West Bernardo Court, Suite 375
San Diego, CA 92127
Telephone: (858) 675-1670
Facsimile: (858) 675-1674

[illegible]

EXAMINER INITIAL		DOCUMENT NUMBER EP 0 935 196 A2	DATE 11/08/1999	COUNTRY Europe	CLASS	SUBCLASS	TRANSLATION	
							YES	NO
		EP 0 849 673 A2	24/06/1998	Europe				
		EP 0 718 757 A2	26/06/1996	Europe				
		EP 0 398 382 A2		Europe				

EXAMINER INITIAL	OTHER DOCUMENTS (INCLUDING AUTHOR, TITLE, DATE, PERTINENT PAGES, ETC.)	
	1.	Microprocessors and Microsystems 20 (1996) 111-123, "The design of a non-blocking load processor architecture", Per Stenstrom et al.
	2.	Hewlett Packard Journal August 1997 "Fully Synthesizable Microprocessor Core via HDL Porting" pp. 107-120, Jim J. Lin
	3.	Electronic Product Design September 1997 "Tuning a customisable risc core for dsp", pp. 19-22
	4.	Universitat Hannover, Germany, "A Core Generator for Fully Synthesizable and Highly Parameterizable Risc-Cores for System-on-Chip Designs, pp. 561-568 with Abstract, M. Berekovic, et al.

DATE CONSIDERED

***EXAMINER:** INITIAL IF CITATION CONSIDERED, WHETHER OR NOT CITATION IS IN CONFORMANCE WITH MPEP 609; DRAW LINE THROUGH CITATION IF NOT IN CONFORMANCE AND NOT CONSIDERED. INCLUDE COPY OF THIS FORM WITH NEXT COMMUNICATION TO APPLICANT.